REMARKS

AND

REASONING ABOUT CITED PRIOR ART

Examiner has cited the following patents/publication as relevant prior art. They are:

A. US-6,316,735, November 2001 to Higashiguchi, Masahiro (Patent).

B. US-6,456,099, September 2002 to Eldridge et al. (Patent).

C. US-5,784,262, July 1998 to Sherman, John V. (Patent).

D. US-2005/0094382, May 2005, to Lassar et al. (Publication)

E. US-6,573,458, June 2003, to Matsubara et al. (Patent).

F. US-6,757,968, July 2004, to Lo et al., (Patent), and

G. US-6,774,474, August 2004, to Caletka et al. (Patent).

Examiner is using the above prior art as the reason for not allowing my claims.

Also, Examiner has used another prior art **patent**, namely **US-6,657,134, to Spielberger et al** for the same reason, but this specific patent was **not** included in the above list. I will address this one as well, later on below.

I agree that some of my original claims do not appear to be novel in light of some of the cited prior art. However, I feel that there are still a number of features in my patent application that are not covered by the prior art.

Consequently, I have amended my claims, so that the new claims cover only material or territory that is not covered by the cited prior art.

I will explain here below, my reasoning, which leads me to believe that the cited Prior Art Patents do not really cover or encroach on my invention and my new claims.

Consequently the cited prior art should not be considered as an obstacle against allowing my new claims.

Based on the above, I would like to respectfully traverse/object to Examiner's findings and rejection.

I will address each one of the seven (7) cited prior art items separately here below.

In paragraph 4 and 5 of Office Action, Examiner has rejected Claims 22-33 and 36-37 as being anticipated by **Eldridge et al.**

This prior art patent was listed in Notice of References Cited, Form PTO-892 as item # **B. US-6,456,099, September 2002 to Eldridge et al.**

So, I will address this one first here below. I will refer to it as "Eldridge".

First, in general, Eldridge does not talk about any thermal center, or fixation point. He does not talk about thermal exposure or thermal deformation and their effect on the solder joints and the system, nor does he talk about the stresses in the solder joints. All these things and the resulting problems are very important. In my invention, I have disclosed solutions to these problems. Eldridge did not, as far as I can see.

Now, I will address the detailed sub-paragraphs of the Office Action, under this main paragraph 5. **I have numbered them as 5.A, 5.B, etc.**

5.A) Regarding claim 22, Examiner remarks that "Because the shape of a bonding pad dictates the solder ball forming on top of it, therefore the pad inherently influence and control the shape and cross-section of the solder pad. Furthermore, the limitation "so as to influence and control ..."is interpreted to only require the ability to so perform. In the case of product claim, only the structure of the claim distinguishes over the prior art." I am grateful to Examiner for drawing my attention to this fact. For this reason, I have cancelled claim 22. I have replaced it by new claims that partially combine several relevant features that were in claims 22 through 26, as you can see in "IN THE CLAIMS".

5.B) Regarding claim 23, two comments. First, I have cancelled this claim and incorporated some of its elements, if relevant, into the new claims.

Second, I wonder whether Examiner would agree with the following interpretation of Eldridge **Fig. 3B**.

In column 2, lines 47-49, Eldridge says: "FIG. 3B is a **logic diagram** of one embodiment of a special contact pad coupled to an **internal circuit node** via a bi-directional **buffer**".

From col 5, line60 through col 6, lines 36, Eldridge explains the difference between the bond pads 110 and the special contact pads 112, especially that "special contact pads 112 may require significantly less supporting circuitry than is typically required by bond pads 110. (See col 6, lines 9-11). The "supporting circuitry" is usually built inside the chip or die, i.e. it can only be "underneath the surface of the chip or die, i.e. inside the die or chip body".

Eldridge goes on in col 6, lines 14-20, and discusses "... electrostatic-discharge (ESD) protection structures such as resistors, capacitors, and/or diodes, latch-up prevention circuitry ... "

And then, in col 6, lines 24-27, he states "For one example, an I/O buffer 120 may be used between an **internal** test point 124 and a special contact pad 110 as shown in FIG. 3B."

Could it be that this FIG. 3B is showing a cross-sectional side view of pad 110 in side view, together with the **internal** circuitry, This **internal** circuitry is shown within the dotted lines of element 120 in FIG. 3B.

It looks as if the rectangle 120, shown with dotted line, is an "electric" diagram of an internal circuit. The rectangular shape 110, above the rectangle 120, would be a side view of the pad 110. So, the rectangle 120 is not a pad, neither a bond pad, nor a special contact pad.

All the pads 110 and 112 in FIG. 3A, as well as in all similar Figures, are shown in top view as "squares"!? I suspect that they are shown "diagrammatically", without really being specific as to their actual geometric shape!?

The following Eldridge Figures show some rectangular shapes, but I don't think they are bonding pads or contact pads, in the sense of what we are talking about here. They are:

In FIG. 1, internal circuits 102, 104 and 106/108 (see col 5, line 61).

In FIG. 2, internal circuits 102, 202 and 106/108.

In FIG. 3A, internal circuits 102, 104 and 106/108.

In FIG. 6, internal circuits 602 and 604.

In FIG. 8, internal circuits 704, 705 and 710.

In FIG. 10, internal circuits 704 and 705.

These rectangular shapes do not represent contact pads, but they represent other elements (internal circuitry or the like) as explained in Eldridge's patent.

Another point re the pads shapes.

In col 1, lines 27-28, Eldridge states: "Typically bond pads sized are on the order of 100 μm (microns)x100 μm (4 milsx4 mils)." Hence, **square** pads.

In col 5, lines 23-27, Eldridge states: "For one embodiment, a bond pad 110 may be approximately 100 μmx100 μm, and a special contact pad may be approximately 5 to 10 μm per side.". Hence, **square** pads.

In col 5, lines 39-41, Eldridge states: "Special contact pads 112 may be formed into an approximately **square** shape, **rectangular** shape, or **any other geometric shape.**"

So, we can not say that Eldridge is showing any specific rectangular contact/bond pads per se. **His pads can be "any other geometric shape".**

Now regarding "alignment".

Then in col 1, lines 28-32, Eldridge continues by stating: "The bond pads are also typically aligned in regular patterns such as peripherally along the outside perimeter of the die, in a grid pattern, or in a column or row generally through the center of the die (lead-on-center)." And so on.

Be it as it may, I have cancelled this claim 23 for now.

5.C) Regarding Claim 24, I guess most of what I have said earlier, regarding claims 22 and 23, applies here too.

5.D) Regarding Claim 25, Examiner states that "the pad is **oriented** in a way that the **short axis is in line with a ray, which start at a fixation point of the device 100 and emanates towards the center of the pad.**" I have tried, but did not succeed in finding where does Eldridge disclose these facts in his patent specifications. I would appreciate it if Examiner can help me here. Thank you.

But again, this may be not so important at this time, since I have cancelled claim 25 as mentioned earlier.

5.E, F, G, and H) Regarding Claim 26, 27, 28 and 29. What I have said earlier above for claim 25 applies to these claims 26 through 29. Basically, it seems to me that the problem is due to the **interpretation of FIG.3B.**

5.A through 5.H) Common note regarding claims 23 through 29. I guess the common objection to all these claims is based on the interpretation of Eldridge FIG. 3B. Once we agree that it does not show a rectangular pad, then the general outlook regarding these claims would change accordingly.

5.I and 5.J) Regarding Claims 30 and 31, Examiner states that in Eldridge "**the pad facing the center point of the device" and "therefore the joint means is also oriented in such a way that the short axis of the joining means cross-section is in line with the ray emanating from the center point (of the device) and reaching towards the center of the joining means cross section**".

I cannot find in Eldridge patent specifications any thing that makes a statement like that.

Could Examiner help me? Thanks.

However, regardless of the wording, I have reworded my claims, so as to clarify what I want to say, and I hope that Examiner will consequently agree that my inventions in these 2 claims are not covered and not anticipated by Eldridge.

5.K and 5.L) Regarding Claims 33 and 34, Examiner is referring to Eldridge Figs. 5 and 15, and to joining means 504/1518/1520. I will address each figure separately. [PS: I believe Examiner wanted to write **Claims 32 and 33, instead of Claims 33 and 34].**

Let me first restate my claims 32 and 33 here.

Claim 32 (New). A joining means as in claim 28, whereby

said joining means **has a generally uniform cross-section along its entire height, to look like a column with uniform cross-section.**

Claim 33 (New). A **joining means** as in claim **28**, whereby said joining means **has a generally uniform cross-section along its entire height, to look like a column with uniform cross-section**, except at the bases where there may be a fillet."

First, Eldridge Fig. 5 shows the joining means 504, which are solder **balls. A ball does not look like a column with uniform cross-section along its entire height.** The cross section of the ball near its center is a "large" circle, while the cross section at any lower height or any higher height would be a "smaller" circle. Hence its cross section is not uniform **along its entire height**. It may look like a circle all right, but the circles at different heights would have different sizes. Hence, not uniform cross section **along its entire height**.

So, if the cross section is uniform along the entire height, then the joining means would not look like a ball, but it would rather look like a "column", as I am saying in my claims 32 and 33.

Accordingly, **Eldridge Fig 5 does not read on my claims 32 and 33.**

Now to Eldridge Fig 15, elements 1518 and 1520.

In column 10, lines 55-59, Eldridge states that the "elements 1518 and 1520 are "**contact balls**" or probes". Also the way they are shown in the Fig. 15 implies that they are round, like **balls** or parts of a **ball**. Eldridge has not specifically stated that they would have "uniform" cross section like columns. And if he states specifically that they are contact "**balls**", then they can not have a uniform cross section. See my explanation above.

So, also **Eldridge Fig 15 does not read on my claims 32 and 33**.

5.M and 5.N) Regarding Claims 36 and 37. As I said earlier above, I have replaced my claim 28 by one or more newer claims, which I have reworded to overcome the objections due to Eldridge. Accordingly, the objections against my claims 36 and 37 will automatically be removed, since they are dependent on claim 28.

So, all the objections due to Eldridge have been removed by the new claims, assuming of course that Examiner will approve my new claims. Consequently, Eldridge cannot be used as a reason to reject my new claims.

Consequently I would like to ask Examiner to allow my case and claims.

In Paragraph 6, 7 and 8 of the Office Action, Examiner combines two prior art patents to reject my claims 34 and 35, which are based on my claim 28. Examiner states that claims 34-35 are rejected under 35 U.S.C. 103(a) as being **unpatentable over Eldridge et al in view of Higashiguchi.**

These two prior art patents were listed in Notice of References Cited, Form PTO-892 as item # **B. US-6,456,099, September 2002 to Eldridge et al.** (already mentioned earlier under my response to paragraphs 4 and 5) and as item **#A. US-6,316,735, November 2001 to Higashiguchi, Masahiro.**

But since Eldridge is out of the picture, as explained above, then the situation now here is different.

I guess that we now have to consider Higashiguchi by itself, as a stand alone prior art.

Based on this assumption, here are my comments.

Higashiguchi has shown in his specification at several points, that having a "solder bump ... having a hand drum shape with a dent in the middle", which I will refer to as the **"hand drum solder bump"**, does provide certain benefits. It reduces the chance of cracking the solder bump under certain conditions. See Higashiguchi from col 6, line 66 to col 7, line 26.

I agree.

Actually, I myself have shown a similar thing in my paper, Ref10. Please see the specification in my patent application, from page 8, line 13 to page 9, line 6, which was published **October 7-9, 1986**. I had written the following in my present patent application:

> "That paper was "Paper #4- "New Solder Column Alloy Improves Reliability of Chip Carrier Assemblies", by Gabe Cherian, Craig Wynn and Harry White, Raychem Corporation, Menlo Park, California, 18th International SAMPE Technical Conference "Materials For Space – The Gathering Momentum", Society for the

Advancement of Material and Process Engineering (SAMPE), Seattle, Washington, **October 7-9, 1986**, pp. 1056-1070."

"This paper shows that a solder column that has a wide base near the pads and a narrower waist about the middle of the height is better suited to withstand the ill effect of the TCE Mismatch between the package and the substrate. The amount of flexing and the level of bending stresses become more favorable with this kind of general shape, than with a column that is uniform in cross section throughout its whole length. I would like to refer to such a shape as the **"starved" column shape**. I will talk more about that further down below."

However, both Higashiguchi and I, at that time, were talking about a solder joint that has a **circular cross section**, mounted on top of a **circular mounting pad**.

Now, in my present invention, I am talking about a different joining means, that has a different shape. My present joining means has an **elongated cross section**, and is mounted on an elongated pad.

In addition, my joining means is **oriented**.

By contrast, Higashiguchi's hand drum solder bump has a circular cross section, and it is mounted on a circular pad. Because of this circular shape of the bump and of the pad, the bump **cannot** be considered as being oriented.

So, I rest my case.

I hope that Examiner would agree with me, that I have a different invention than that of Higashiguchi's, based on the above remarks and explanations, and on the stated differences and distinctions. I feel that my invention is different than Higashiguchi's, and that Higashiguchi does not teach what I am proposing/disclosing in my invention. So, there should be no reason to deny my claims due to Higashiguchi's patent.

Consequently, Higashiguchi's prior art patent cannot be considered as an obstacle against my claims. I would like to respectfully ask Examiner to strike out Higashiguchi's patent as a reason for rejecting my claims, and I would like to ask Examiner to allow my case and claims.

In Paragraph 9, of the Office Action, Examiner listed a number of prior art patents and a publication, as being made of record and not relied upon, and as being pertinent to applicant's disclosure. I will now address each one of them here below, in the order they were listed in paragraph 9. **I have numbered them as 9.A, 9.B, etc.**

9.A) Examiner has stated that "**Caletka et al (6,774,474) disclose a partially captured oriented interconnections for BGA packages and a method of forming the interconnections.**"

This prior art patent was listed in Notice of References Cited, Form PTO-892 as item # **G. US-6,774,474, August 2004, to Caletka et al.**

First, Caletka is providing a very clever way to overcome the high "**shear**" stresses that are induced in "his" solder joints.

Conventional pads, which are round and non-oriented, create solder joints that are stubby and short in their height in the vertical direction perpendicular to the general surface of the BGA and the PCB. These assemblies and their solder joints, when exposed to thermal cycling and the resulting linear dimensional changes in the BGA and the PCB, stress the solder joints mostly under "shear". Also part of the linear deformation could cause the solder joint to "rotate" or "roll" between the BGA and the PCB. Some people say that this would cause a "torsion/torque" action into the solder joint, which would cause the solder joint to "roll" in the direction of the linear deformation.

One way to prevent this rolling of the solder joint is to do what Caletka has done here. It is a very clever way to try to solve the problem of "fatigue life". It also helps in solving the "wiring space within the package".

However, there are other ways to solve the problem of "fatigue life". One such way is the way that I have disclosed in my present invention.

There are **two major differences** between Caletka and my invention.

The **first major difference**, and actually the most important one, is **the direction or orientation of the solder pads and the solder joints. Caletka's orientation is exactly the opposite of my orientation.**

The **second major difference** is **the height of the solder joints. Caletka's solder joints are short and stubby, resulting from his use of solder balls, while my joints are tall and slender.**

I will first talk about the height of the joints.

In the specification of my present patent application, I have listed a number of articles or white papers and certain US Patents, and I have given them Reference Numbers. I have included them in this present patent application. I will highlight a few of them here.

Ref8. Paper #2- "BGA Mounting and Chip Scale Packaging". This was included in Ref6, pages OC-A-43 through –49.

Ref9. Paper #3- "BGA Mounting Using Improved Solder Columns". This was included in Ref6, pages OC-A-50 through –56.

Ref15. US Patent # 4,664,309, dated May 12, 1987, entitled "CHIP MOUNTING DEVICE"; Inventors: Leslie J. Allen, Gabe Cherian and Stephen H. Diaz; Assignee: Raychem Corp., Menlo Park, Calif.

Ref16. US Patent # 4,705,205, dated November 10, 1987, entitled "CHIP CARRIER MOUNTING DEVICE"; Inventors: Leslie J. Allen, Gabe Cherian and Stephen H. Diaz; Assignee: Raychem Corp., Menlo Park, Calif.

In all the above references, I have disclosed that the "columns" are a better form of solder joints than the stubby, short solder joints obtained when reflowing solder balls of conventional BGAs.

The main reason of all this is that "tall" "column-like" solder joints get stressed substantially under **"bending"** stress. This is in contrast to the "shear" stress that prevails in the case of short, stubby solder joints, which are obtained when the BGA solder balls are reflowed.

So, I am providing "tall" "column-like" solder joints, which are stressed predominantly under bending. In the case of bending stresses, I can control the level of stress by properly selecting the height of the column and the cross section of the column, i.e. diameter or width and length of the cross section.

So, one of the big differences between Caletka and my invention is that Caletka's solder joints are relatively short and stubby, while my solder joints are tall and slender and "column-like".

Second, I will talk about the orientation of the joints.

In yet other References and in the specification of the present patent application, I have talked about the "oriented leads of packages" and the benefits of using them, over the "conventional orthogonal" leads of similar kinds of packages.

And more importantly, I have shown in the present invention, how to accomplish this objective, i.e. how to control the "orientation" of the leads and of the columns.

I have disclosed that I prefer that each column be oriented such that it presents the "least resistance against **bending/flexing** in the direction of the linear deformation at the location of that specific solder joint". This can be accomplished by orienting the joint cross section such that its short axis be in line with the ray emanating from the thermal center of the package and reaching out to the center of that specific column's cross section.

This makes it that my column's cross section would be oriented at 90 degrees with respect to the orientation of Caletka solder joints.

In other words, Caletka orientation is very bad if his solder joints were to be as tall as mine and are under "BENDING" stresses. They will be in the worst orientation. But if we consider short stubby solder joints, like those of Caletka, which are under "SHEAR" stresses, then they would be OK.

So, without going into any more detailed differences between Caletka and my invention, we can see that there are enough differences already, which indicate that Caletka does not read on my invention, and thus, it can not be used as a reason to reject my invention and claims.

Consequently, I would like to respectfully ask Examiner to strike out Caletka patent as a reason for rejecting my claims, and I would like to ask Examiner to allow my case and claims.

9.B) Examiner stated that **"Lo et al (6,757,968) disclose a chip scale packaging on CTE matched printed wiring boards."**

This prior art patent was listed in Notice of References Cited, Form PTO-892 as item #F-**US-6,757,968, July 2004, to Lo et al.,**

I am not sure which parts of Lo's patent is relevant to Examiner. So, I will assume that they are what I will discuss here below. If Examiner has other parts in mind, please advise and I will respond accordingly. Thanks.

Lo talks about three layers of attachments, using solder or other materials.

The **first** layer of solder attachment is between the integrated circuit die 24 and the first printed wiring board 22, **or as he called it the redistribution board 22,** to create the chip scale package assembly 14. I will refer to this as the chip scale package assembly or the **chip assembly 14,** or **the first sub-assembly.** I will also refer to this layer of **solder** as the **chip side solder**.

The **second** layer of attachment is between the heat sink layer 16 and the second printed wiring board 18, to create what I will refer to as the heat sink assembly 12, or **the second sub-assembly.** The attachment material can be solder or other materials, so I will refer to this attachment as the **second attachment material.**

The **third** layer of attachment is between the two previous sub-assemblies, i.e. between the chip assembly 14 and the heat sink assembly 12. This final step creates the final assembly, which I will refer to as the **total assembly.** I will refer to this third attachment layer as the **third attachment solder.**

I am assuming that Examiner's statement refers to the **chip scale packaging on CTE matched printed wiring boards**, i.e. the first layer of solder attachment between the integrated circuit die 24 and the first printed wiring board 22, to create the **chip assembly 14,** or **the first sub-assembly**. I will address this part of Lo's patent.

However, the following statements could lead me to believe that Examiner may also refer to the **third attachment solder.**

Response Remarks:

Lo states in the lower portion of the Abstract that "the circuit pads on the **first** printed wiring board **(first sub-assembly)** may have solder balls formed of **high temperature** solder that do not melt when the **heat sink** assembly is assembled **with chip scale** package assembly **(third attachment)**. The solder balls allow chip scale package assembly **to maintain a predetermined distance** from the circuit pads on the **second (???)** printed wiring board." The words in parentheses are inserted by me for clarification. This statement is confusing to me. How can the solder balls **inside** the first sub-assembly maintain the distance **underneath** it, i.e. the distance between the first sub-assembly and the second sub-assembly?

Lo also states in col 3, lines38-39, that "Die pads 28 are preferably coupled to circuit pads 26 by a high temperature solder." Now, this refers to what I have called the **chip side solder, i.e. the first sub-assembly.**

Again in col 3, lines 62 …, he repeats statements to the same meaning. Etc.

However, in Col 4, lines 8-12, Lo states "Preferably, a solder or adhesive having a lower temperature than that previously applied to circuit pads 26 is used. **This allows the balls formed of the high temperature solder on circuit pads 32 to hold integrated circuit die 24 at a constant distance from printed wiring board 18.**"

Again, this last sentence is a little bit **confusing** to me, like the statement in the Abstract. Which high temp solder is holding a constant distance between die 24 and printed wiring board 18? As we have seen above, there are **two different layers of solder** between **circuit die 24 and the printed wiring board 18.** The **first** layer of solder balls is between die 24 and the first wiring board/redistribution layer 22, which I have called the chip side solder, i.e. **within the first sub-assembly,** and the **second** layer of solder balls is **between the first sub-assembly and the second sub-assembly,** which I have called the third attachment solder layer. So, which layer of solder balls is Lo talking about?

Nevertheless, I will address the point both ways.

It seems to me that the whole point of contention and discussion is that the high melt temp solder will **hold integrated circuit die 24 at a constant distance from printed wiring board 18. Let's first look at the first step, i.e. the distance between the chip 24 and the redistribution board 22.**

The solder balls are said to be high melt temp solder. It is true that such high temp solder balls will hold a constant distance between the attached devices, **but** so will any other solder balls or most any other attachment material. The only difference here is that the high melt temp solder balls will not melt during the subsequent reflow operation. This is commonly known in the industry as "**fire down**" procedure. You always try to do the early operations at a temp that is high enough, higher than the expected temps of subsequent operations, so that during these subsequent operations, you do not destroy the results of the preceding operations.

The solder for the subsequent operation, i.e. the **third attachment solder** between the first and second sub-assemblies, may **also** be a high melt temp solder, but it could have a melting temp that is still **lower** than that of the previous high melt temp solder used within the first sub-assembly. **This condition would also hold the components at a constant distance from each other.**

So, what is the point?

I guess that the difference between Lo's approach and my invention, is that I am using at least three different methods to **positively** hold constant the distance between the attached components and not relying only on the behavior of the solder itself. And all these methods are different from Lo's.

I will discuss each one separately here below.

The **first approach** is illustrated by my Fig. 29A and 29B.

Fig. 29A shows a solder ball with a core, which has a higher melting temp than the melting temp of the outside layer. Let's say the core as being a copper ball, and the outside layer as being the meltable solder. During reflow, the outside solder will melt and become

"liquidy". It will wet the solder pads which are on the two components that are being soldered together. Let's say these components as being a BGA on top and a PCB at the bottom. The BGA will fall down, under its own weight or by a predetermined load/force, and ultimately will rest on top of the copper ball. It could also be floating on top of the molten solder. By properly selecting the volume of solder in advance, we can ensure that the solder will first wet the two solder pads (of the PCB and of the BGA) and will then create an acceptable solder joint. Furthermore, by again properly selecting the volume of solder in advance, we can ensure that the solder joint will be "starved", i.e. will have the hour glass shape that is shown in Fig. 29B. This has been described in detail in my present patent application specification, in pages 75-76, under "1- Use Cored Solder Balls, or Conventional Solder Balls with Stand-Offs".

A **second approach** to hold the distance constant between the two components being attached together is shown in Fig. 30. I call it the method "using an external stand-off". It is shown in Fig. 30A through Fig. 30G. It is also described in detail in my present patent application specification pages 77 through 84, under the title "3- Use Controlled Volume Preform and Individual/Separate Stand-Offs".

The **third approach** is shown in Figs. 31 through 33, and I have covered it in my present patent application specification, in pages 86 through 87, under the title of "4- Shape Memory Method".

One final comment about Lo. The fact that Lo's patent covers chip scale packaging **on CTE matched printed wiring boards,** makes it even less of an obstacle against my invention. In my invention, neither the wiring boards nor the other components need to be CTE matched. In fact, the benefit of my invention is that it can solve the same case as that of Lo, **and in addition**, it can solve cases with CTE mismatch, which are more problematic. My invention would improve the reliability and operating life of such assemblies, even if and especially when those assemblies have components with different CTEs.

So, without going into any more detailed differences between Lo and my invention, we can see that there are enough differences already, which indicate that Lo does not read on my invention, and thus, it can not be used as a reason to reject my invention and claims.

Consequently, I would like to respectfully ask Examiner to strike out Lo patent as a reason for rejecting my claims, and I would like to ask Examiner to allow my case and claims.

9.C) Examiner stated that "**Spielberger et al (6, 657,134) disclose a stacked ball grid array**."

This prior art patent was **not** listed in Notice of References Cited, Form PTO-892.

I am not sure which parts of **Spielberger**'s patent is relevant to Examiner. So, I will assume that they are what I will discuss here below. If Examiner has other parts in mind, please advise and I will respond accordingly. Thanks.

Once again, I would like to thank Examiner for uncovering all these prior art patents. They are at once gratifying and at the same time, they are helpful to me, giving me examples of how to write my claims.

Spielberger once again confirms what I had talked about almost 20 years ago. He elaborates on the subject in his column 1, line 64 all the way to col 2, line 22. Besides the "hourglass" shape, he also talks about the use of two different solder alloys, namely the 90/10 Pb/Sn solder and the eutectic 63/37 Sn/Pb solder.

In my above response to Paragraph 6, 7, 8 and to Higashiguchi's patent, I had mentioned Ref10 of my present patent application. That Ref10 was a paper that I have presented at a SAMPE Conference, **October 7-9, 1986**, in Seattle, Washington, USA. In that Ref10, I had stated, in essence, that "a solder column that has a wide base near the pads and a narrower waist about the middle of the height is better suited to withstand the ill effect of the TCE Mismatch between the package and the substrate". I have supported that statement by appropriate stress analysis. This matches pretty closely what Spielberger is saying in his patent, which issued on Dec. 2, 2003. Interestingly enough, I had also used these two solder alloys in my product that I had described in the above Ref10 paper.

However, this Spielberger patent, although very clever and probably very effective, is still **not a reason to object to my claims** in my present invention. Let me explain.

First, Spielberger is using "... an "**interposer**" between an electronic component and a printed circuit board ... "as stated in his column 2, lines 49-50 and as seen obviously in practically all his figures. In his Abstract, Spielberger calls it "**stress relief substrate**".

In all his claims, Spielberger calls it "**flexible stress relief substrate.**" See his independent claim 1, in col 6, line6, his independent claim 10, in col 6, line 64, his independent claim 18, in col 7, line 59, and his independent claim 22, in col 8, line 38. All his other claims depend from these 4 independent claims, and do not change that expression about this interposer.

By contrast, I do **not** have such an interposer in my present invention.

Second, in conjunction with his use of this interposer, Spielberger is using **two rows of solder balls**. The **first row** by the top surface of the interposer and the **second row** by the bottom surface of the interposer.

By contrast, I do **not** have two such rows in my present invention, but I have **only one row of solder joints**.

Third, Spielberger has succeeded in creating a quasi solder "column", by stacking two solder balls on top of each other, as in his Fig. 6. He has also succeeded in configuring the solder column to have an approximate "hourglass shape" as in his Fig. 7. Excellent. However, he accomplished this by stacking two independent solder balls one on top of the other, and by having the interposer and a number of interconnecting elements and pads between these two balls.

By contrast, I do not have any similar arrangement. I use only one solder joint between my two electronic components, for example, between the BGA and the PCB. And I do not have the interposer and other elements stuck in the middle of the column.

Fourth and most importantly, Spielberger does not talk anywhere in his patent about "**orientation**". All his conductive vias and connection pads are round (circular in shape). See

for example, his Fig. 2, which shows them as circles. See also his claims 4, 5, 13, 14, 20 and 21, where he mentions the sizes of the **diameters** of these pads. The solder balls are obviously circular also. Any shape that is circular, like these pads and balls, **cannot be oriented**. Besides, Spielberger has **never mentioned anything** implying that he intended to orient his solder joints.

By contrast, one of the main features of my invention is the **"orientation"** of my solder joints, as obvious in my drawings, specification and claims.

So again, without going into any more detailed differences between Spielberger and my invention, we can see that there are enough differences already, which indicate that Spielberger does not read on my invention, and thus, it can not be used as a reason to reject my invention and claims.

Consequently, I would like to respectfully ask Examiner to strike out Spielberger patent as a reason for rejecting my claims, and I would like to ask Examiner to allow my case and claims.

9.D) Examiner stated that "**Matsubara et al (US 6,573,458) disclose a printed circuit board**."

This prior art patent was listed in Notice of References Cited, Form PTO-892, as item # **E. US-6,573,458, June 2003, to Matsubara et al. (Patent).**

I am not sure which parts of **Matsubara's** patent is relevant to Examiner. So, I will assume that they are what I will discuss here below. If Examiner has other parts in mind, please advise and I will respond accordingly. Thanks. I am guessing that Examiner intends to compare Matsubara with my **Figures 29A and 29B**.

Matsubara's main feature is the "**ball-shaped terminals**" as described in his claims and his figures.

I will paraphrase from **Matsubara's claim 1**, which is a good representation of all his other claims.

In claim 1, starting at column 8, line 25, Matsubara states that "a plurality of ball-shaped **terminals (A)** provided on a major surface of said board member, said ball-shaped terminals each comprising: **a pad (B) disposed on said major surface** of said board member; **a full spherical metallic ball (C)** adapted to be engaged by **a socket terminal (D)** formed by a pair of ball receiving members which, taken together, are of a semispherical form; **a brazing metal (E)** brazing said metallic ball onto said pad; and **gold plating layer formed on a surface of said metallic ball (F)**, ... , and **the metallic ball having a diameter greater than that of the pad (G)** and being brazed on the pad substantially coaxially therewith."

I have added the letter in parentheses, for easy referencing.

I will show here below the **differences** between Matsubara and my invention.

My Figures 29A and 29B show a **solder joint** between two devices, **not** a terminal **(A)** on a major surface of said board member, i.e. on one side only as in Matsubara, and it is **not** intended to interface with a socket terminal **(D)**.

My solder joint starts with a **solder ball** that has a core of a high temp melting material, which could be copper. The core could be another material. It is **not brazed (E)** to the pads. The solder ball's solder **fully surrounds the core.** It is **not** a metallic ball that will be gold plated **(F).**

And most importantly, my solder joint does not have a **diameter greater than that of the pad (G). If the diameter of my solder ball is greater than that of the pad that it is attached to, then the solder joint would not work as intended.** It would defeat the purpose and would act against the whole intention of the invention. **My solder ball, as seen in Figs. 29A and 29B has a diameter that is obviously smaller than the pads** of either of the two components being soldered together.

And when we consider that ultimately we want that the solder joints have an **hourglass shape,** then it becomes more obvious still, that the diameter of my solder joint at such mid-height of the joint and of the core should be smaller than the pads on the two components to be soldered together.

Matsubara's terminals do not have the hourglass shape.

Lastly, Matsubara's terminals are not oriented.

So again, without going into any more detailed differences between Matsubara and my invention, we can see that there are enough differences already, which indicate that Matsubara does not read on my invention, and thus, it can not be used as a reason to reject my invention and claims.

Consequently, I would like to respectfully ask Examiner to strike out Matsubara patent as a reason for rejecting my claims, and I would like to ask Examiner to allow my case and claims.

9.E) Examiner stated that "**Lassar et al (US-2005/0094382) disclose a connection pad layout.**"

This prior art **Publication** was listed in Notice of References Cited, Form PTO-892, as item **# D. US-2005/0094382, May 2005, to Lassar et al. (Publication)**

When I saw the figure of the front sheet of this patent, I got scared. I thought that this prior art could be damaging to my invention. But, upon closer examination of the specification and claims, and all the figures, I realized that this Lassar patent is no reason for rejecting my invention and my claims, as will be seen here below.

I guess that Examiner, looking at the "curved" row of pads in the Abstract figure and Figures 2, 3, 4 and 6, got the same impression that I got at the beginning. So, I will address this prior art and show that it does not read on my invention.

I will first give a general overview of the **differences** between Lassar and my invention, and then go into some finer details.

The whole purpose of Lassar is to "**accommodate the terminals of an interconnect that may be warped**" (Lassar page 3, paragraph 0037, lines 10-11).

Lassar explains that purpose, in different words and in more details, in his page 3, paragraph 0034, describing the warped interconnect as due to "**a manufacturing tolerance, or deviation**". He continues by saying that the connection pads layouts are designed to accommodate these warped interconnect. In other words, instead of throwing away the **warped (defective) interconnects**, they re-design the layout of the connection pads on the substrate assembly, so that they can utilize the defective interconnects.

I guess that they need to go through the procedure illustrated by Fig. 7, for every "batch" of interconnect that they make. After the batch is manufactured, they inspect the interconnects and determine the amount, magnitude, seriousness, etc of the warpage, and then (I guess) they take the "average" for that batch and then they design/re-design the "new"

appropriate position and configuration of the connection pads on the substrate assembly, to accommodate the warpage of this specific batch of interconnects. Again, I guess that they would have to repeat this whole process for every batch of interconnects that they manufacture.

So, in other words, the way I understand it, is that they make "matched sets" of substrate assemblies for every new batch of interconnects that gets manufactured.

I guess that this is still more cost effective for them, than throwing away some of those interconnects that are warped too much to fit on "standard" substrate assemblies. I am sure that they know what they are doing.

However, how does this affect my invention?

I would say, not at all.

It is obvious from studying the whole patent document, that the warpage of the interconnects is **not consistent and not repeatable**. Consequently, the solutions used by Lassar to accommodate these warpages are also not consistent and not repeatable. In other words, once they have a specific design, they can not apply it to ALL interconnects and/or ALL substrate assemblies. In other words, they do not have one "standard" design applicable to ALL cases. They have to "custom tailor" each batch, to suit the specific conditions of that specific batch. To prove this point, I refer to Figs. 3, 5 and 6.

In Fig. 3, Lassar is showing two arrays of connection pads. Array 302 shows a relatively uniform curvature, implying that the warpage is consistent. However, array 306 shows a strange configuration. Array 306 has two regions. Region 314 is a straight line, while region 316 is curved. In page 2, paragraph 0023, Lassar states: "... array 302 is laid out such that the connection pads 304 each align with the terminals of an interconnect that is **warped on both ends**. Connection pad array 306 is laid out such that the connection pads 308 align with the terminals of an interconnect that is **straight on one end** (aligns with connection pads 308 in

region 314) **and** that is **warped on the other end** (aligns with connection pads 308 in region 316)".

The gist of all the above is that this warpage is not consistent or repeatable. And the configuration of the connection pads is simply trying to accommodate it. And this changes from case to case, depending on random manufacturing outcomes. The configuration of the connection pads has to be re-designed each time to accommodate the situation at that time.

By contrast, in my invention, the configuration of the contact pads is governed by certain rules of physics. They intend to counteract the ill effects of the linear deformation, resulting from the expansion and contraction of the components of the assemblies, when exposed to thermal cycling and/or fluctuations. These linear deformations follow well known patterns and rules of physics, that are consistent and repeatable. And the configuration of the contact pads has to follow those well known patterns and rules, otherwise the whole purpose of the invention gets lost.

Other points to support my point of view.

If we look at the substrate assembly 300 in Lassar Fig. 3, we can see that the curvature of array 302 is such that the center of curvature is way out, outside the rectangle representing the substrate 300. Usually, the center of curvature of such pads arrays would be the "thermal center" of the device in question. The center of curvature of array 302, which can be conceived by looking at Lassar Fig. 3, can not be the "thermal center" of the substrate. Normally, the thermal center of any body/member lies roughly fairly close to its "geometric center", unless the member is not homogeneous, in which case the thermal center would be offset slightly from the geometric center. But in either case, the thermal center is usually within the contour or perimeter of the body, not far outside the body. It is almost inconceivable to have a thermal center for such a substrate 300, as shown in Fig. 3, at a position close to the center of curvature of this array 302. So, this is another indication that

the configuration of these contact pads is not intended to accommodate the thermal deformation of the components.

And looking at the array 306, we can not conceive of a case where one part of the member would have some thermal deformation in region 316, while it has no thermal deformation in region 314. What would be the reason to have one region (316) curved, and the other region (314) straight, if both regions are exposed to the same thermal fluctuations?

Furthermore, by looking at Lassar Fig. 5, we see that the connection pads are not curved or oriented at all. Lassar simply "extends" the pads sideways, up and down, to take care of his problem. This would not solve any thermal deformation problems like in the case of my invention.

Besides, Lassar has not mentioned anything in his specification that implies that he intended to accommodate any thermal deformation.

So one more time, without going into any more detailed differences between Lassar and my invention, we can see that there are enough differences already, which indicate that Lassar does not read on my invention, and thus, it can not be used as a reason to reject my invention and claims.

Consequently, I would like to respectfully ask Examiner to strike out Lassar patent as a reason for rejecting my claims, and I would like to ask Examiner to allow my case and claims.

9.F) Examiner stated that "**Sherman (US-5,784,262) discloses an arrangement of pads and through-holes for semiconductor packages.**"

This prior art Patent was listed in Notice of References Cited, Form PTO-892, as item # C. US-5,784,262, July 1998 to Sherman, John V. (Patent).

Again, by looking at the figure on the front page of Sherman patent, I first got the impression that some danger is lurking. However, after studying the patent closely, I realized that there is no reason to fear.

Sherman's patent is intended to pack more features in less space. He does not have any inkling about the thermal fluctuations and their effects and has no intentions of doing anything about that. But, as Examiner had stated earlier in his Office Action, the intent is not the governing factor. His exact words are: "only the structure of the claim distinguishes over the prior art". So, I will discuss the structure of Sherman's claims and his specifications.

Sherman's claim 1 states: "An arrangement of **mounting pads (A)** on a substrate **(B)** for connection with electrical contacts, comprising: a plurality of segments **(C)**, a first segment **(D)** of said plurality having a plurality of the mounting pads **(E)** in a first row **(F)**; and each of said first row mounting pads **(G)** in connection with **(H)** an **offset through-hole (I) oriented (J) outwardly (K) in a first direction (L) that is substantially parallel (M) to a first bisector (N) for said first segment (O).**" The letters in parentheses are inserted for easy referencing.

Let's analyze what Sherman is saying in his claim 1.

The mounting pads **(A) (E) (G)** are grouped **(D)** in segments **(C)**. Each segment has a bisector **(N)**, which has a certain direction **(P)** (a certain angle with respect to an axis of some sort). **See Note 1.**

Each mounting pad **(G)** is "in connection with" **(H)** an "offset through-hole" **(I)**. **See Note 2.**

The offset through-hole is "oriented" **(J). See Note 3.**

The orientation is outwardly **(K)** in a first direction **(L)**, that is substantially parallel **(M)** to the direction **(P)** of the bisector **(N). See Note 4.**

Note 1: The **direction** of the Sherman's bisector **is constant.** In Sherman's patent, it seems that this direction is at 45 degrees with respect to the main axes. This direction is **not** changing. It is **not like the rays representing the thermal deformation at different points, as in my invention.** The directions of these rays changes and varies depending on the location of every specific point in question, on the surface of the components being attached together.

Note 2: Looking at Sherman's Figs. 2A and 2B, and to his specifications column 4, lines 59-65, we can see that the mounting pads (item 18A) are connected to the through-hole pad or short via pad (item 26A) by an interconnection trace (item 27A). Sherman calls this whole thing the "**pad-through-hole combination**" **(item 21A')**. So, this is what Sherman means in his claim 1, where items G, H and I, are connected together to create his "**pad-through-hole combination" (item 21A')**. See above.

Note 3: In his claim 1, Sherman says that the offset through-hole is oriented. I don't think that he really means that. I guess that he really means that the "**pad-through-hole combination" (item 21A'), as seen in a top view drawing,** will look as if it is oriented. We can argue that this is a point of semantics. True. But I just wanted to point it out.

Note 4: The orientation of the "**pad-through-hole combination" (item 21A'), as seen in a top view drawing,** is in the direction of the bisector. We have already said in Note 1 above that the direction of the bisector is constant and it does not address the thermal deformation issue. So consequently, the direction of these "**pad-through-hole combination" (item 21A'), as seen in a top view drawing,** in turn, **does not address the thermal deformation issue either.**

Now, let's look at Sherman's second independent claim, claim 4. His last paragraph states: "wherein each of said second and third rows has an outermost mounting pad in

connection with an offset through-hole **oriented outwardly in a direction other than said first direction**." And looking at Sherman's Fig. 7, we can see an example of what he means. He explains his intentions in col 8, lines 8-48. He closes by saying "... allow for extra trace routing clearance."

This is the clincher. If Sherman were interested in orienting his features to take care of the thermal effects, by orienting his "inner" rows in a certain direction, then **how come he changes that direction for the "outer" rows?** It does not compute.

In spite of all the above, we don't want to overlook a more and very important fact.

As seen in Sherman's Fig. 1, the BGA 10 is attached to the PCB 20 **by soldering the solder balls 14 to the mounting pads 18 ONLY. Neither the "through-hole pads or short via pads (item 26A)" nor the "interconnection traces (item 27A)" enter into the picture, when he solders the BGA to the PCB.** So, all the above discussion is academic.

I repeat, the interconnections between the BGA and the PCB occur ONLY on top of the mounting pads 18. These mounting pads 18 are round and hence can not be oriented.

The mounting pads 18A are **circular**, as seen in the figures, and the solder balls 14a-14d are **ball-shaped leads** (Sherman Col 4, line39). Sherman goes on and states in col 4, lines 42-44 "Leads 14a-14d can take some other shape, as long as the leads can be electrically connected to corresponding mounting pads." So, again, **Sherman does not talk about, nor does he specify, any mounting pads of any particular shape, and obviously he does not talk about, nor does he specify, any specific "orientation" to those mounting pads.**

So, in summary, Sherman has no intentions of solving the problems arising from the thermal cycling effects. And his mounting pads are either circular or "can have any particular shape", and he has no intentions of orienting his solder joint. The proof is clear from all the above discussions.

So one last time, without going into any more detailed differences between Sherman and my invention, we can see that there are enough differences already, which indicate that Sherman does not read on my invention, and thus, it can not be used as a reason to reject my invention and claims.

Consequently, I would like to respectfully ask Examiner to strike out Sherman patent as a reason for rejecting my claims, and I would like to ask Examiner to allow my case and claims.

Accordingly and based on all my above explanations, I believe that the Examiner will agree with me that the cited patents and publication do not really create an obstacle in the way of allowing all my proposed new/amended claims.

Consequently, I respectfully request that all my new/amended claims be allowed and that a patent be granted to me. Thank you in advance.

Thank you in advance and best regards.

Gabe Cherian

Gabe Cherian.